

AMENDMENTS TO THE CLAIMS

Please enter the following amendments.

Claims 1-5 (Cancelled)

6. (Currently Amended) A method of manufacturing a silicon wafer, comprising the steps of:

A) (a) pulling up a single silicon crystal ingot from a silicon melt ~~by controlling~~
~~V/G~~; and

B) (b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G (°C/mm) is a temperature gradient at an interface between said ingot and silicon melt;

wherein said pulling-up of said ingot at the step (a) is carried out is pulled-up such that V/Ga and V/Gb become 0.23 to 0.50 mm²/minute °C, respectively, where V (mm/minute) is a pulling-up speed, and both of V/Ga and V/Gb exceeding a first critical ratio ((V/G)₁) for restricting vacancy agglomerates to a vacancy point defect dominant domain at the center of said ingot;

where Ga (°C/mm) is an axial temperature gradient at the center of said ingot and Gb (°C/mm) is an axial temperature gradient at the edge of said ingot at temperatures in a range of 1,300°C to a melting point of silicon;

wherein said heat treatment of said silicon wafer at step (c) is carried out in a 100% hydrogen atmosphere, a mixed atmosphere of hydrogen and nitrogen at temperatures in a range of 1,050°C to 1,220°C for 30 to 150 minutes;

resulting in that the number of crystal originated particles smaller than 0.12 μm in the wafer surface is restricted to a range of 3 to 10 pieces/cm²; and the number of crystal originated particles of 0.12 μm or greater in the wafer surface becomes 0.5 pieces/cm² or less.

Claims 7-22 (Cancelled)

23. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G ($^{\circ}\text{C}/\text{mm}$) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a second critical ratio $((V/G)_2)$ for avoiding occurrence of agglomerates of interstitial silicon point defects; and equal to or less than a third critical ratio $((V/G)_3)$ for restricting agglomerates of vacancy point defects within a center domain dominated by vacancy point defects;

wherein said sliced silicon at the step (b) wafer includes no crystal originated particles nor dislocation pits in the surface of said silicon wafer, and is a silicon wafer in which oxidation induced stacking faults actualize only in a disk shape at the center of said silicon wafer unlike the ring shape, when said silicon wafer was heat treated in an oxygen atmosphere at temperatures of $1,000^{\circ}\text{C} \pm 30^{\circ}\text{C}$ for 2 to 5 hours and subsequently heat treated at temperatures of $1,130^{\circ}\text{C} \pm 30^{\circ}\text{C}$ for 1 to 16 hours;

wherein said heat treatment of said silicon wafer at the step of (c) is carried out in an atmosphere of 100% oxygen or in a mixed atmosphere of oxygen and nitrogen at temperatures of $1,130^{\circ}\text{C}$ to $1,200^{\circ}\text{C}$ for 1 minute to 6 hours; resulting in obtaining a silicon wafer which is free of crystal originated particles and of oxidation induced stacking faults, when said silicon wafer was heat treated by said oxidation-induced-stacking-fault-actualizing heat treatment.

24. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G ($^{\circ}\text{C}/\text{mm}$) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal, to or greater than a second critical ratio $((V/G)_2)$ for avoiding occurrence of agglomerates of interstitial silicon point defects; and equal to or less than a third critical ratio $((V/G)_3)$ for restricting agglomerates of vacancy point defects within a center domain dominated by vacancy point defects;

wherein said sliced silicon wafer at the step (b) includes no crystal originated particles nor dislocation pits in the surface of said silicon wafer, and is a silicon wafer in which oxidation induced stacking faults actualize only in a disk shape at the center of said silicon wafer unlike the ring shape, when said silicon wafer was heat treated in a oxygen atmosphere at temperatures of $1,000^{\circ}\text{C} \pm 30^{\circ}\text{C}$ for 2 to 5 hours and subsequently heat treated at temperatures of $1,130^{\circ}\text{C} \pm 30^{\circ}\text{C}$ for 1 to 16 hours;

wherein said heat treatment of said silicon wafer at the step (c) is carried out in an atmosphere of 100% argon at temperatures of $1,130^{\circ}\text{C}$ to $1,200^{\circ}\text{C}$ for 1 minute to 6 hours; resulting in obtaining a silicon wafer which is free of crystal originated particles and of oxidation induced stacking faults, when said silicon wafer was heat treated by said oxidation-induced-stacking-fault-actualizing heat treatment.

25. (New) A method of manufacturing a silicon wafer, comprising the steps of:

- (a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G ;
- (b) slicing said ingot into a silicon wafer; and
- (c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G ($^{\circ}\text{C}/\text{mm}$) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a second critical ratio $((V/G)_2)$ for avoiding occurrence of agglomerates of interstitial silicon point defects; and equal to or less than a third critical ratio $((V/G)_3)$ for restricting agglomerates of vacancy point defects within a center domain dominated by vacancy point defects;

wherein said sliced silicon wafer at the step (b) includes no crystal originated particles nor dislocation pits in the surface of said silicon wafer, and is a silicon wafer in which oxidation induced stacking faults actualize only in a disk shape at the center of said silicon wafer unlike the ring shape, when said silicon wafer was heat treated in a oxygen atmosphere at

temperatures of $1,000^{\circ}\text{C}\pm 30^{\circ}\text{C}$ for 2 to 5 hours and subsequently heat treated at temperatures of $1,130^{\circ}\text{C}\pm 30^{\circ}\text{C}$ for 1 to 16 hours;

wherein said heat treatment of said silicon wafer at the step (c) is carried out in an atmosphere of 100% hydrogen or in a mixed atmosphere of hydrogen and argon at temperatures of $1,150^{\circ}\text{C}$ to $1,250^{\circ}\text{C}$ for 1 minute to 4 hours; resulting in providing a silicon wafer which is free of crystal originated particles and of oxidation induced stacking faults, when said silicon wafer was heat treated by said oxidation-induced-stacking-fault-actualizing heat treatment.

26. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G ($^{\circ}\text{C}/\text{mm}$) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held in the range from a fifth critical ratio $((V/G)_5)$ to a sixth critical ratio $((V/G)_6)$, the range corresponding to the domain [OSF] for forming OSF nuclei;

wherein said sliced silicon wafer at the step (b) includes no crystal originated particles nor dislocation pits in the surface of said silicon wafer, and is a silicon wafer in which oxidation induced stacking faults are generated only in a disk shape at the center of said silicon wafer, unlike the ring shape, in 25% or more of the entire area of said silicon wafer and oxygen precipitations accompanied with no dislocation generation is generated at a density of 1×10^5 to 3×10^7 pieces/ cm^2 , when said silicon wafer was heat treated in an oxygen atmosphere at temperatures of $1,000^{\circ}\text{C}\pm 30^{\circ}\text{C}$ for 2 to 5 hours and subsequently heat treated at temperatures of $1,130^{\circ}\text{C}\pm 30^{\circ}\text{C}$ for 1 to 16 hours;

wherein said heat treatment of said silicon wafer at the step (c) is carried out in a hydrogen gas atmosphere or in an atmosphere including hydrogen gas from a room temperature up to $1,100^{\circ}\text{C}$ to $1,250^{\circ}\text{C}$ at a temperature elevating speed of $3^{\circ}\text{C}/\text{minute}$ to $150^{\circ}\text{C}/\text{second}$;

wherein said heat-treated silicon wafer is held for 1 minute to 2 hours followed by leaving said silicon wafer at a room temperature; resulting in that a denuded zone is formed over a depth of 1 to 100 μm from the wafer surface, to thereby provide said silicon wafer having a

BMD density of 2×10^4 to 2×10^8 pieces/cm³ in a portion deeper than said denuded zone and exhibiting an IG effect.

27. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G (°C/mm) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a fourth critical ratio ((V/G)₄) for avoiding occurrence of agglomerates of interstitial silicon point defects; and equal to or less than a fifth critical ratio ((V/G)₅) for restricting agglomerates of vacancy point defects to the ingot center domain dominated by vacancy point defects;

wherein said sliced silicon wafer at the step (b) comprises a mixed domain of [P_v] and [P_i] and has an oxygen concentration of 0.8×10^{18} to 1.4×10^{18} atoms/cm³ (old ASTM),

where [P_i] is a domain neighboring with a domain [I] dominated by interstitial silicon point defects, is classified into a perfect domain [P] including no agglomerates of point defects, and has a concentration of interstitial silicons lower than the lowest concentration of interstitial silicons capable of forming interstitial dislocations, and

where [P_v] is a domain neighboring with a domain [V] dominated by vacancy point defects, is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

wherein said heat treatment of said silicon wafer at the step (c) comprises the steps of:

conducting a first step heat treatment for holding said silicon wafer in an atmosphere of nitrogen, hydrogen, oxygen, mixture of nitrogen and argon, mixture of hydrogen and argon or a mixture of oxygen and argon at temperatures of 600°C to 850°C for 120 to 250 minutes; and

subsequently conducting a second step heat treatment for rapidly heating said silicon wafer in a hydrogen gas or in an atmosphere including a hydrogen gas from a room

temperature up to temperatures of 1,100°C to 1,250°C at a temperature elevating speed of 3 °C/minute to 150 °C/second, and for holding said silicon wafer for 1 minute to 2 hours followed by leaving said silicon wafer at a room temperature; resulting in that a denuded zone is formed over a depth of 1 to 100 μm from the wafer surface, to thereby provide said silicon wafer having a BMD density of 2×10^4 to 2×10^8 pieces/ cm^3 in a portion deeper than said denuded zone and exhibiting an IG effect.

28. (New) A method of manufacturing a silicon wafer comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G (°C/mm) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a fourth critical ratio $((V/G)_4)$ for avoiding occurrence of agglomerates of interstitial silicon point defects; and equal to or less than a fifth critical ratio $((V/G)_5)$ for restricting agglomerates of vacancy point defects to the ingot center domain dominated by vacancy point defects;

wherein said sliced silicon wafer at the step (b) comprises one or both of a domain $[P_V]$ and a domain $[P_I]$ and has an oxygen concentration of 1.2×10^{18} atoms/ cm^3 or more (old ASTM),

where, in said single silicon crystal ingot,

said domain $[P_I]$ is a domain neighboring with a domain $[I]$, is classified into a perfect domain $[P]$, and has a concentration of interstitial silicons lower than the lowest concentration of interstitial silicons capable of forming interstitial dislocations,

said domain $[P_V]$ is a domain neighboring with a domain $[V]$, is classified into said perfect domain $[P]$, and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

said domain $[I]$ is a domain dominated by interstitial silicon point defects,

said domain $[V]$ is a domain dominated by vacancy point defects, and

said perfect domain [P] includes no agglomerates of interstitial silicon point defects and no agglomerates of vacancy point defects;

wherein said heat treatment of said silicon wafer at the step (c) comprises the steps of: heating said silicon wafer in an atmosphere of a hydrogen gas or an argon gas from a room temperature up to temperatures of 900°C to 1,200°C at a temperature elevating speed of 5 to 50 °C/minute; and

holding said silicon wafer for 5 to 120 minutes, to thereby conduct a first step heat treatment followed by leaving said silicon wafer at a room temperature; resulting in that a denuded zone is formed over a depth of 1 to 5 μm from the wafer surface, to thereby provide said silicon wafer having a BMD density of 2×10^4 to 2×10^8 pieces/ cm^3 in a portion deeper than said denuded zone and exhibiting an IG effect.

29. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G (°C/mm) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a critical point; and equal to or less than a fifth critical ratio $((V/G)_5)$ for restricting agglomerates of vacancy point defects to the ingot center domain dominated by vacancy point defects;

wherein said sliced silicon wafer at the step (b) comprises a domain $[P_v]$ and has an oxygen concentration of 1.2×10^{18} atoms/ cm^3 or more (old ASTM),

where, in said single silicon crystal ingot,

said domain $[P_v]$ is a domain neighboring with a domain [V], is classified into a perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

said domain [V] is a domain dominated by vacancy point defects, and

said perfect domain [P] includes no agglomerates of interstitial silicon point defects and no agglomerates of vacancy point defects;

wherein said heat treatment of said silicon wafer at the step (c) comprises the steps of:

heating said silicon wafer in an atmosphere of a hydrogen gas or an argon gas from a room temperature up to temperatures of 900°C to 1,200°C at a temperature elevating speed of 5 to 50 °C/minute;

holding said silicon wafer for 5 to 120 minutes, to thereby conduct a first step heat treatment;

introducing said silicon wafer in a nitrogen atmosphere or in an oxidative atmosphere from a room temperature into a furnace at temperatures of 500°C to 800°C;

heating said silicon wafer up to temperatures of 750°C to 1,100°C at a temperature elevating speed of 10 to 50 °C/minute; and

holding said silicon wafer for 4 to 48 hours, to thereby conduct a second step heat treatment followed by leaving said silicon wafer at a room temperature; resulting in that a denuded zone is formed over a depth of 1 to 5 μm from the wafer surface, to thereby provide said silicon wafer having a BMD density of 2×10^4 to 2×10^8 pieces/ cm^3 in a portion deeper than said denuded zone and exhibiting an IG effect.

30. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G (°C/mm) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a fourth critical ratio $((V/G)_4)$ for avoiding occurrence of agglomerates of interstitial silicon point defects; and equal to or less than a critical point; or V/G is held at a value which is: equal to or greater than said fourth critical ratio $((V/G)_4)$; and equal to or less than a fifth critical ratio $((V/G)_5)$ for restricting agglomerates of vacancy point defects to the ingot center domain dominated by vacancy point defects;

wherein said sliced silicon wafer at the step (b) comprises a domain [P_I] or comprises a mixed domain including said domain [P_I] and a domain [P_V] and has an oxygen concentration of 1.2×10^{18} atoms/cm³ or more (old ASTM),

where, in said single silicon crystal ingot,

said domain [P_I] is a domain neighboring with a domain [I], is classified into a perfect domain [P], and has a concentration of interstitial silicons lower than the lowest concentration of interstitial silicons capable of forming interstitial dislocations,

said domain [P_V] is a domain neighboring with a domain [V], is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

said domain [I] is a domain dominated by interstitial silicon point defects,

said domain [V] is a domain dominated by vacancy point defects, and

said perfect domain [P] includes no agglomerates of interstitial silicon point defects and no agglomerates of vacancy point defects;

wherein said heat treatment of said silicon wafer at the step (c) comprises the steps of:

heating said silicon wafer in an atmosphere of a hydrogen gas or an argon gas from a room temperature up to temperatures of 900°C to 1,200°C at a temperature elevating speed of 5 to 50 °C/minute;

holding said silicon wafer for 5 to 120 minutes, to thereby conduct a first step heat treatment;

introducing said silicon wafer in a nitrogen atmosphere or in an oxidative atmosphere from a room temperature into a furnace at temperatures of 400°C to 700°C;

heating said silicon wafer up to temperatures of 800 to 1,100°C at a temperature elevating speed of 0.5 to 10 °C/minute; and

holding said silicon wafer for 0.5 to 40 hours, to thereby conduct a second step heat treatment followed by leaving said silicon wafer at a room temperature; resulting in that a denuded zone is formed over a depth of 1 to 5 μm from the wafer surface, to thereby provide said silicon wafer having a BMD density of 2×10^4 to 2×10^8 pieces/cm³, in a portion deeper than said denuded zone and exhibiting an IG effect.

31. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and ($^{\circ}\text{C}/\text{mm}$) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a critical point; and equal to or less than a sixth critical ratio $((V/G)_6)$ corresponding to a domain [OSF] for forming OSF nuclei;

wherein said sliced silicon wafer at the step (b) comprises a mixed domain of a domain [OSF] and a domain $[P_V]$, and has an oxygen concentration of 1.2×10^{18} atoms/cm³ or more (old ASTM),

where, in said single silicon crystal ingot,

said domain [OSF] is classified into a domain [V], and OSF's are to generate in said domain [OSF] when said ingot in a silicon wafer state is subjected to a thermal oxidization treatment,

said domain $[P_V]$ is a domain neighboring with a domain [V], is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

said domain [V] is a domain dominated by vacancy point defects, and

said perfect domain [P] includes no agglomerates of interstitial silicon point defects and no agglomerates of vacancy point defects;

wherein said heat treatment of said silicon wafer at the step (c) comprises the steps of:

heating said silicon wafer in an atmosphere of a hydrogen gas or an argon gas from a room temperature up to temperatures of 900°C to $1,200^{\circ}\text{C}$ at a temperature elevating speed of 5 to $50^{\circ}\text{C}/\text{minute}$;

holding said silicon wafer for 5 to 120 minutes, to thereby conduct a first step heat treatment followed by leaving said silicon wafer at a room temperature; resulting in that a denuded zone is formed over a depth of 1 to 5 μm from the wafer surface, to thereby provide said silicon wafer having a BMD density of 2×10^4 to 2×10^8 pieces/ cm^3 in a portion deeper than said denuded zone and exhibiting an IG effect.

32. (New) A method of manufacturing a silicon wafer, comprising the steps of:

(a) pulling up a single silicon crystal ingot from a silicon melt by controlling V/G;

(b) slicing said ingot into a silicon wafer; and

(c) heat treating said silicon wafer;

where V (mm/minute) is a pulling-up speed, and G ($^{\circ}\text{C}/\text{mm}$) is a temperature gradient at an interface between said ingot and silicon melt;

wherein V/G at the step (a) is held at a value which is: equal to or greater than a critical point; and equal to or less than a sixth critical ratio $((V/G)_6)$ corresponding to a domain [OSF] for forming OSF nuclei;

wherein said sliced silicon wafer at the step (b) comprises a mixed domain of a domain [OSF] and a domain [P_V], and has an oxygen concentration of 1.2×10^{18} atoms/ cm^3 or more (old ASTM),

where, in said single silicon crystal ingot,

said domain [OSF] is classified into a domain [V] and OSF's are to generate in said domain [OSF] when said ingot in a silicon wafer state is subjected to a thermal oxidization treatment,

said domain [P_V] is a domain neighboring with a domain [V], is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

said domain [V] is a domain dominated by vacancy point defects, and

said perfect domain [P] includes no agglomerates of interstitial silicon point defects and no agglomerates of vacancy point defects;

wherein said heat treatment of said silicon wafer at the step (c) comprises the steps of:

heating said silicon wafer in an atmosphere of a hydrogen gas or an argon gas from a room temperature up to temperatures of 900°C to 1,200°C at a temperature elevating speed of 5 to 50 °C/minute;

holding said silicon wafer for 5 to 120 minutes, to thereby conduct a first step heat treatment;

introducing said silicon wafer in a nitrogen atmosphere or in an oxidative atmosphere from a room temperature into a furnace at temperatures of 500°C to 800°C;

heating said silicon wafer up to temperatures of 750°C to 1,100°C at a temperature elevating speed of 10 to 50 °C/minute; and

holding said silicon wafer for 4 to 48 hours, to thereby conduct a second step heat treatment followed by leaving said silicon wafer at a room temperature; resulting in that a denuded zone is formed over a depth of 1 to 5 μm from the wafer surface, to thereby provide said silicon wafer having a BMD density of 2×10^4 to 2×10^8 pieces/ cm^3 in a portion deeper than said denuded zone and exhibiting an IG effect.